

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of -

SAITO et al.

Application Number: To be Assigned

Filed: Concurrently Herewith

For: SEMICONDUCTOR DEVICE

ATTORNEY DOCKET NO. HITA.0501

**Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231**

INFORMATION DISCLOSURE STATEMENT

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, this Information Disclosure Statement is submitted in the above-identified patent application. A listing of documents to be published on the face of any patent granted from this application is submitted herewith on Form PTO-1449. Any other documents or information submitted for consideration by the Examiner are listed in this paper. A copy of each U.S. and foreign patent, or each publication or portion thereof listed or herein identified, is submitted herewith.

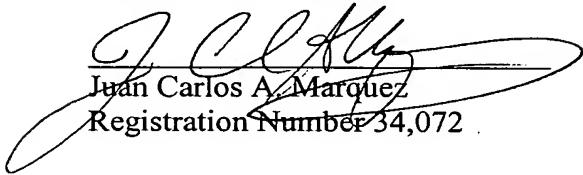
This Information Disclosure Statement is submitted with the initial filing of the application. Accordingly, no fee is due or payable at this time.

The Examiner is requested to acknowledge consideration of the information provided in this paper in accordance with prescribed procedures.

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	APPLICANT SAITO et al	
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U.S. Patent Documents

Examiner Initial	DOCUMENT NUMBER	DATE	NAME	CLA SS	SUBC LASS	FILING DATE

Foreign Patent Documents

Examiner Initial	DOCUMENT NUMBER	FILING DATE	COUNTRY	CLASS	SUB- CLA SS	TRANSLATION	
						YES	NO
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		D.A. Buchanan et al. "80 nm Poly-silicon Gated n-FETs with Ultra-Thin Al ₂ O ₃ Gate Dielectric for ULSI Applications", IEEE (2000), 4 pages
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